

# DATA SHEET

**74LVC162373A; 74LVCH162373A**  
16-bit D-type transparent latch with  
30  $\Omega$  series termination resistors;  
5 V input/output tolerant; 3-state

Product specification  
File under Integrated Circuits, IC24

1999 Aug 05

# 16-bit D-type transparent latch with 30 $\Omega$ series termination resistors; 5 V input/output tolerant; 3-state

## 74LVC162373A; 74LVCH162373A

### FEATURES

- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V
- 5 V tolerant input/output for interfacing with 5 V logic
- Wide supply voltage range of 1.2 to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH162373A only)
- High impedance when  $V_{CC} = 0$
- Power off disables outputs, permitting live insertion.

### DESCRIPTION

The 74LVC(H)162373A is a 16-bit D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. One latch enable (LE) input and one output enable ( $\overline{OE}$ ) are provide for each octal. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 and 5 V environment.

The 74LVC(H)162373 consists of 2 sections of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the  $D_n$  inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When  $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state off latches.

The 74LVCH162373A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

The 74LVC(H)162373A is designed with 30  $\Omega$  series termination resistors in both HIGH and LOW output stages to reduce line noise.

### FUNCTION TABLE (per section of eight bits)

See note 1.

| OPERATION MODES                             | INPUTS          |    |       | INTERNAL LATCHES | OUTPUTS        |
|---|-----------------|----|-------|------------------|----------------|
|   | $\overline{OE}$ | LE | $D_n$ |                  | $Q_0$ to $Q_7$ |
| Enable and read register (transparent mode) | L               | H  | L     | L                | L              |
|   | L               | H  | H     | H                | H              |
| Latch and read register                     | L               | L  | l     | L                | L              |
|   | L               | L  | h     | H                | H              |
| Latch register and disable outputs          | H               | L  | l     | L                | Z              |
|   | H               | L  | h     | H                | Z              |

### Note

1. H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
L = LOW voltage level;  
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
Z = high-impedance OFF-state.

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**QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

| SYMBOL            | PARAMETER   | CONDITIONS                                     | TYPICAL    | UNIT     |
|-------------------|---|--|------------|----------|
| $t_{PHL}/t_{PLH}$ | propagation delay<br>D <sub>n</sub> to Q <sub>n</sub><br>LE to Q <sub>n</sub> | $C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$ | 3.2<br>3.5 | ns<br>ns |
| $C_I$             | input capacitance   |  | 5.0        | pF       |
| $C_{PD}$          | power dissipation capacitance per latch                                       | $V_{CC} = 3.3\text{ V}$ ; note 1               | 26.0       | pF       |

**Note**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts.

**ORDERING INFORMATION**

| OUTSIDE NORTH AMERICA | NORTH AMERICA  | PACKAGE                       |      |         |          |          |
|-----------------------|----------------|-------------------------------|------|---------|----------|----------|
|                       |                | TEMPERATURE RANGE             | PINS | PACKAGE | MATERIAL | CODE     |
| 74LVC162373ADL        | VC162373A DL   | -40 to +85 $^{\circ}\text{C}$ | 48   | SSOP    | plastic  | SOT370-1 |
| 74LVC162373ADGG       | VC162373A DGG  |                               | 48   | TSSOP   | plastic  | SOT362-1 |
| 74LVCH162373ADL       | VCH162373A DL  |                               | 48   | SSOP    | plastic  | SOT370-1 |
| 74LVCH162373ADGG      | VCH162373A DGG |                               | 48   | TSSOP   | plastic  | SOT362-1 |

**PINNING**

| PIN                            | SYMBOL                         | DESCRIPTION                      |
|--------------------------------|--------------------------------|----------------------------------|
| 1                              | $1\overline{\text{OE}}$        | output enable input (active LOW) |
| 2, 3, 5, 6, 8, 9, 11, 12       | $1\text{Q}_0$ to $1\text{Q}_7$ | data inputs/outputs              |
| 4, 10, 15, 21, 28, 34, 39, 45  | GND                            | ground (0 V)                     |
| 7, 18, 31, 42                  | $V_{CC}$                       | DC supply voltage                |
| 13, 14, 16, 17, 19, 20, 22, 23 | $2\text{Q}_0$ to $2\text{Q}_7$ | data inputs/outputs              |
| 24                             | $2\overline{\text{OE}}$        | output enable input (active LOW) |
| 25                             | 2LE                            | latch enable input (active HIGH) |
| 36, 35, 33, 32, 30, 29, 27, 26 | $2\text{D}_0$ to $2\text{D}_7$ | data inputs                      |
| 47, 46, 44, 43, 41, 40, 38, 37 | $1\text{D}_0$ to $1\text{D}_7$ | data inputs                      |
| 48                             | 1LE                            | latch enable input (active HIGH) |

16-bit D-type transparent latch with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

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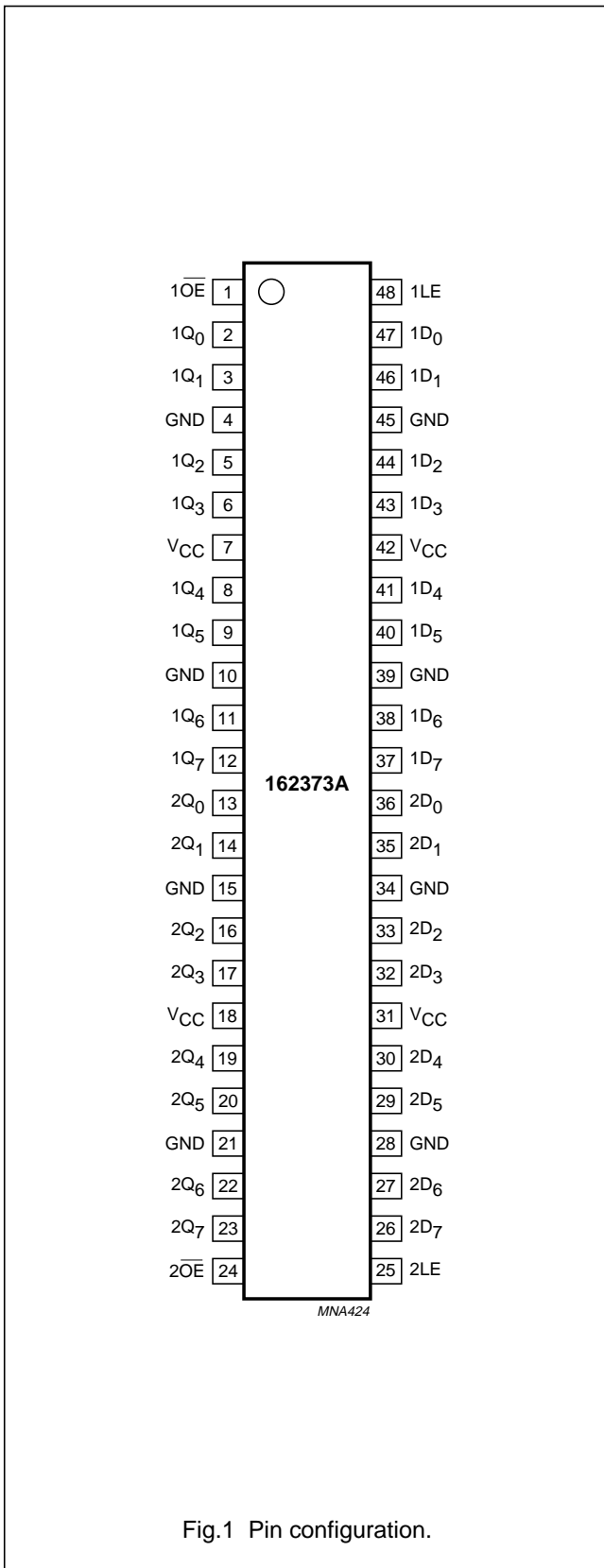


Fig.1 Pin configuration.

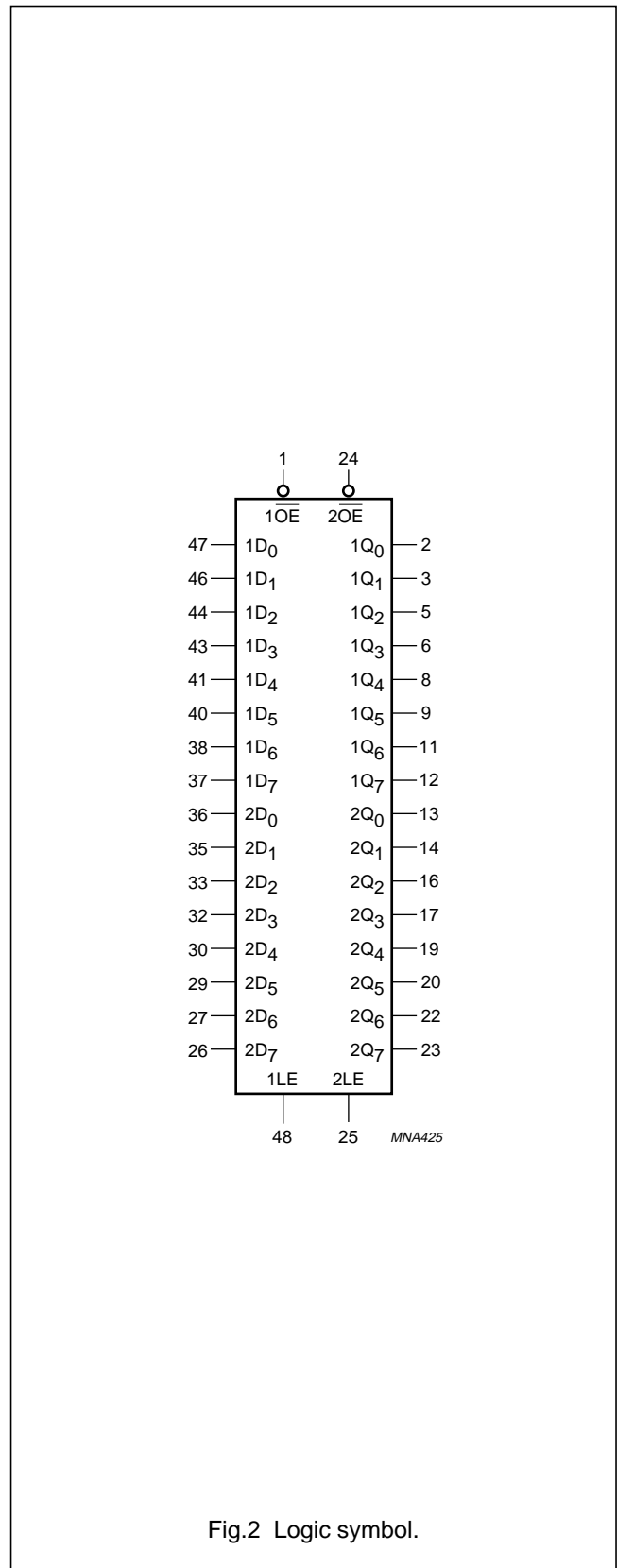


Fig.2 Logic symbol.

16-bit D-type transparent latch with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

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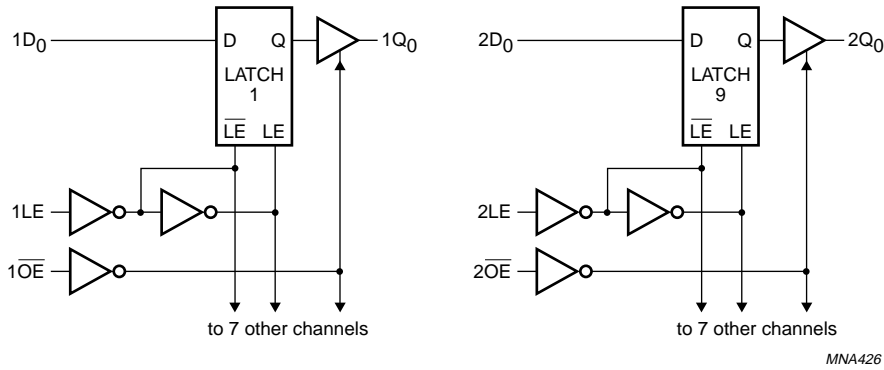


Fig.3 Logic diagram.

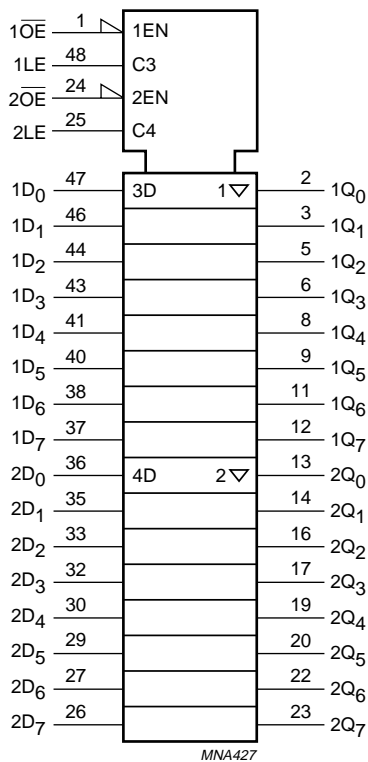


Fig.4 IEC logic symbol.

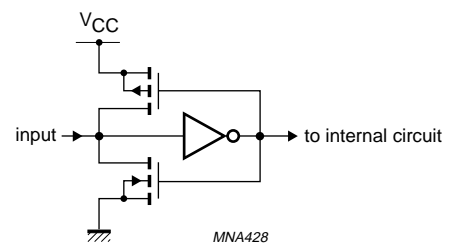


Fig.5 Bus hold circuit.

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#### RECOMMENDED OPERATING CONDITIONS

| SYMBOL     | PARAMETER   | CONDITIONS                               | LIMITS |          | UNIT               |
|------------|---|--|--------|----------|--------------------|
|            |   |  | MIN.   | MAX.     |                    |
| $V_{CC}$   | DC supply voltage<br>for max. speed performance<br>for low-voltage applications |  | 2.7    | 3.6      | V                  |
|            |   |  | 1.2    | 3.6      | V                  |
| $V_I$      | DC input voltage range  |  | 0      | 5.5      | V                  |
| $V_O$      | DC output voltage range<br>output HIGH or LOW state<br>3-state                  |  | 0      | $V_{CC}$ | V                  |
|            |   |  | 0      | 5.5      | V                  |
| $T_{amb}$  | operating ambient temperature   | see DC and AC characteristics per device | -40    | +85      | $^{\circ}\text{C}$ |
| $t_r, t_f$ | input rise and fall times   | $V_{CC} = 1.2$ to $2.7$ V                | 0      | 20       | ns/V               |
|            |   | $V_{CC} = 2.7$ to $3.6$ V                | 0      | 10       | ns/V               |

#### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

| SYMBOL            | PARAMETER   | CONDITIONS  | MIN. | MAX.           | UNIT               |
|-------------------|---|---|------|----------------|--------------------|
| $V_{CC}$          | DC supply voltage   |   | -0.5 | +6.5           | V                  |
| $I_{IK}$          | DC input diode current                                      | $V_I < 0$   | -    | -50            | mA                 |
| $V_I$             | DC input voltage  | note 1  | -0.5 | +5.5           | V                  |
| $I_{OK}$          | DC output diode current                                     | $V_O > V_{CC}$ or $V_O < 0$                               | -    | $\pm 50$       | mA                 |
| $V_O$             | DC output voltage<br>output HIGH or LOW<br>output 3-state   | note 1<br>note 1  | -0.5 | $V_{CC} + 0.5$ | V                  |
|                   |   |   | -0.5 | +6.5           | V                  |
| $I_O$             | DC output diode current                                     | $V_O = 0$ to $V_{CC}$                                     | -    | $\pm 50$       | mA                 |
| $I_{CC}, I_{GND}$ | DC $V_{CC}$ or GND current                                  |   | -    | $\pm 100$      | mA                 |
| $T_{stg}$         | storage temperature   |   | -65  | +150           | $^{\circ}\text{C}$ |
| $P_{tot}$         | power dissipation plastic shrink mini-pack (SSOP and TSSOP) | above 60 $^{\circ}\text{C}$ derate linearly with 5.5 mW/K | -    | 500            | mW                 |

#### Note

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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### DC CHARACTERISTICS

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

| SYMBOL                   | PARAMETER   | TEST CONDITIONS  |                     | T <sub>amb</sub> (°C) |                     |          | UNIT    |
|--------------------------|---|--|---------------------|-----------------------|---------------------|----------|---------|
|                          |   | OTHER  | V <sub>CC</sub> (V) | -40 to +85            |                     |          |         |
|                          |   |  |                     | MIN.                  | TYP. <sup>(1)</sup> | MAX.     |         |
| V <sub>IH</sub>          | HIGH-level input voltage                            |  | 1.2                 | V <sub>CC</sub>       | –                   | –        | V       |
|                          |   |  | 2.7 to 3.6          | 2.0                   | –                   | –        |         |
| V <sub>IL</sub>          | LOW-level input voltage                             |  | 1.2                 | –                     | –                   | GND      | V       |
|                          |   |  | 2.7 to 3.6          | –                     | –                   | 0.8      |         |
| V <sub>OH</sub>          | HIGH-level output voltage                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –6 mA           | 2.7                 | V <sub>CC</sub> – 0.5 | –                   | –        | V       |
|                          |   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>I <sub>O</sub> = –100 $\mu$ A | 3.0                 | V <sub>CC</sub> – 0.2 | V <sub>CC</sub>     | –        |         |
|                          |   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –12 mA          | 3.0                 | V <sub>CC</sub> – 0.8 | –                   | –        |         |
| V <sub>OL</sub>          | LOW-level output voltage                            | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6 mA            | 2.7                 | –                     | –                   | 0.40     | V       |
|                          |   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100 $\mu$ A     | 3.0                 | –                     | –                   | 0.20     |         |
|                          |   | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12 mA           | 3.0                 | –                     | –                   | 0.55     |         |
| I <sub>I</sub>           | input leakage current                               | V <sub>I</sub> = 5.5 V or GND; note 2  | 3.6                 | –                     | $\pm$ 0.1           | $\pm$ 5  | $\mu$ A |
| I <sub>OZ</sub>          | 3-state output OFF-state current                    | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>V <sub>O</sub> = 5.5 V or GND | 3.6                 | –                     | 0.1                 | $\pm$ 5  | $\mu$ A |
| I <sub>off</sub>         | power off leakage supply                            | V <sub>I</sub> or V <sub>O</sub> = 5.5 V   | 0.0                 | –                     | 0.1                 | $\pm$ 10 | $\mu$ A |
| I <sub>CC</sub>          | quiescent supply current                            | V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0                            | 3.6                 | –                     | 0.1                 | 20       | $\mu$ A |
| $\Delta$ I <sub>CC</sub> | additional quiescent supply current per control pin | V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0                           | 2.7 to 3.6          | –                     | 5                   | 500      | $\mu$ A |
| I <sub>BHL</sub>         | bus hold LOW sustaining current                     | V <sub>I</sub> = 0.8 V; notes 3, 4 and 5   | 3.0                 | 75                    | –                   | –        | $\mu$ A |
| I <sub>BHH</sub>         | bus hold HIGH sustaining current                    | V <sub>I</sub> = 2.0 V; notes 3, 4 and 5   | 3.0                 | –75                   | –                   | –        | $\mu$ A |
| I <sub>BHLO</sub>        | bus hold LOW overdrive current                      | V <sub>I</sub> = 0.8 V; notes 3, 4 and 6   | 3.6                 | 500                   | –                   | –        | $\mu$ A |
| I <sub>BHHO</sub>        | bus hold HIGH overdrive current                     | V <sub>I</sub> = 0.8 V; notes 3, 4 and 6   | 3.6                 | –500                  | –                   | –        | $\mu$ A |

### Notes

1. All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. For bus hold parts, the bus hold circuit is switched off when V<sub>I</sub> exceeds V<sub>CC</sub> allowing 5.5 V on the input terminal.
3. Valid for data inputs of bus hold parts (LVCH162373-A) only.
4. For data inputs only, control inputs do not have a bus hold circuit.
5. The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input state.

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### AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $T_{amb} = -40$  to  $+85$  °C.

| SYMBOL            | PARAMETER   | WAVEFORMS         | LIMITS                                     |                     |      |                          |      | UNIT |
|-------------------|---|-------------------|--|---------------------|------|--------------------------|------|------|
|                   |   |                   | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ |                     |      | $V_{CC} = 2.7 \text{ V}$ |      |      |
|                   |   |                   | MIN.                                       | TYP. <sup>(1)</sup> | MAX. | MIN.                     | MAX. |      |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>nD <sub>n</sub> to nQ <sub>n</sub> | see Figs 6 and 10 | 1.5  | 3.3                 | 5.4  | 1.5                      | 6.4  | ns   |
|                   | nLE to nQ <sub>n</sub>                                  | see Figs 7 and 10 | 1.5  | 3.5                 | 5.8  | 1.5                      | 6.8  | ns   |
| $t_{PZH}/t_{PZL}$ | 3-state output enable time<br>nOE to nQ <sub>n</sub>    | see Figs 9 and 10 | 1.5  | 4.0                 | 7.3  | 1.5                      | 8.3  | ns   |
| $t_{PHZ}/t_{PLZ}$ | 3-state output disable time<br>nOE to nQ <sub>n</sub>   | see Figs 9 and 10 | 1.5  | 3.4                 | 4.8  | 1.5                      | 5.8  | ns   |
| $t_W$             | nLE pulse width HIGH                                    | see Fig.7         | 4.0  | 2.0                 | –    | 3                        | –    | ns   |
| $t_{su}$          | set-up time nD <sub>n</sub> to nLE                      | see Fig.8         | +2.0                                       | –0.1                | –    | 1.7                      | –    | ns   |
| $t_h$             | hold time nD <sub>n</sub> to nLE                        | see Fig.8         | 1.5  | 0.1                 | –    | 1.2                      | –    | ns   |

#### Note

1. Typical values at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25$  °C.



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AC WAVEFORMS

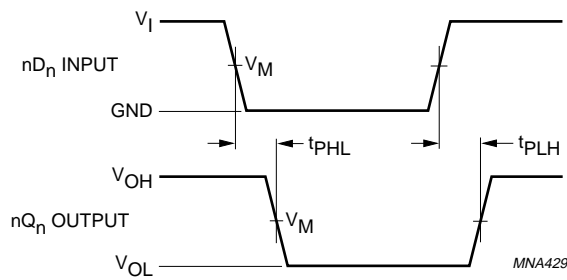


Fig.6 The input (nD<sub>n</sub>) to output (nQ<sub>n</sub>) propagation delay.

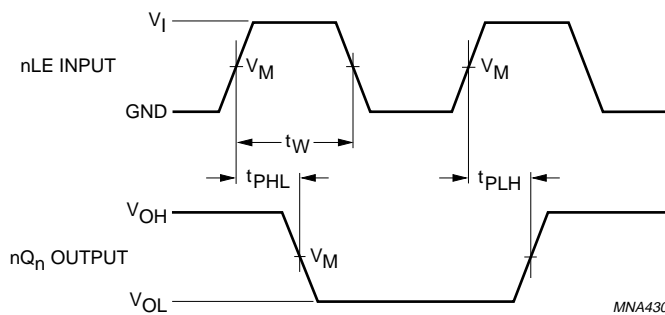
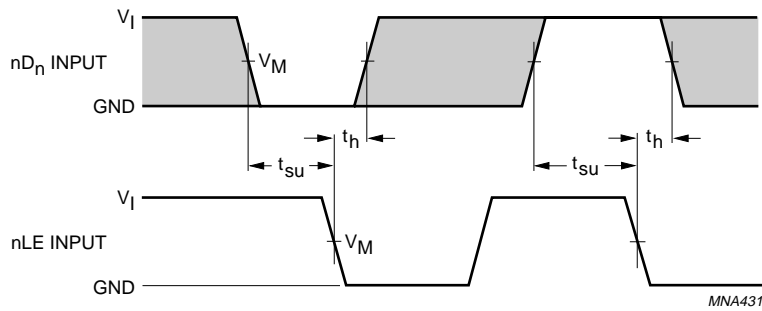


Fig.7 Latch enable input (nLE) pulse width, the latch enable input to output (nQ<sub>n</sub>) propagation delays.

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The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.8 Data set-up and hold times for the nD<sub>n</sub> input to the nLE input.

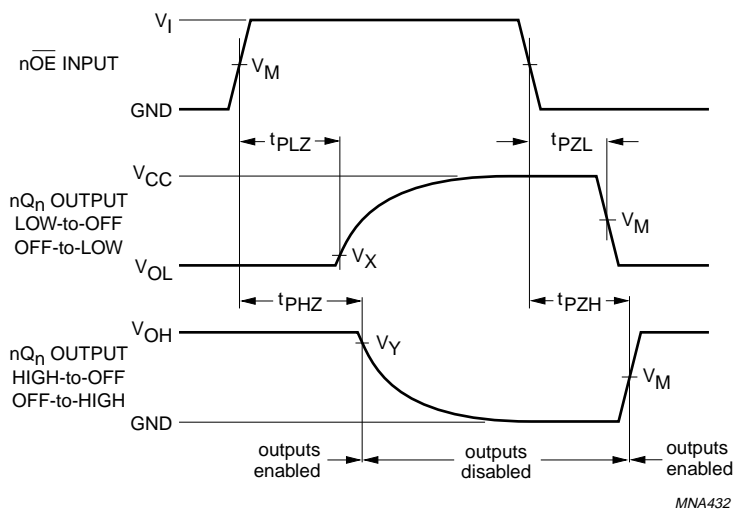
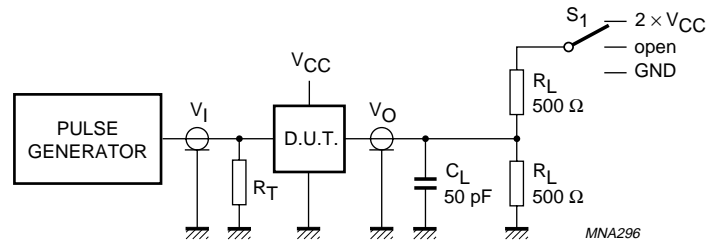


Fig.9 3-state enable and disable times.

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| TEST                               | S <sub>1</sub>      |
|------------------------------------|---------------------|
| t <sub>PLH</sub> /t <sub>PHL</sub> | open                |
| t <sub>PLZ</sub> /t <sub>PZL</sub> | 2 × V <sub>CC</sub> |
| t <sub>PHZ</sub> /t <sub>PZH</sub> | GND                 |

| V <sub>CC</sub> | V <sub>I</sub>  |
|-----------------|-----------------|
| <2.7 V          | V <sub>CC</sub> |
| 2.7 - 3.6 V     | 2.7 V           |

Definitions for test circuit:

R<sub>L</sub> = Load resistor; see Chapter "AC characteristics".

C<sub>L</sub> = Load capacitance including jig and probe capacitance (see Chapter "AC characteristics").

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.10 Load circuitry for switching times.

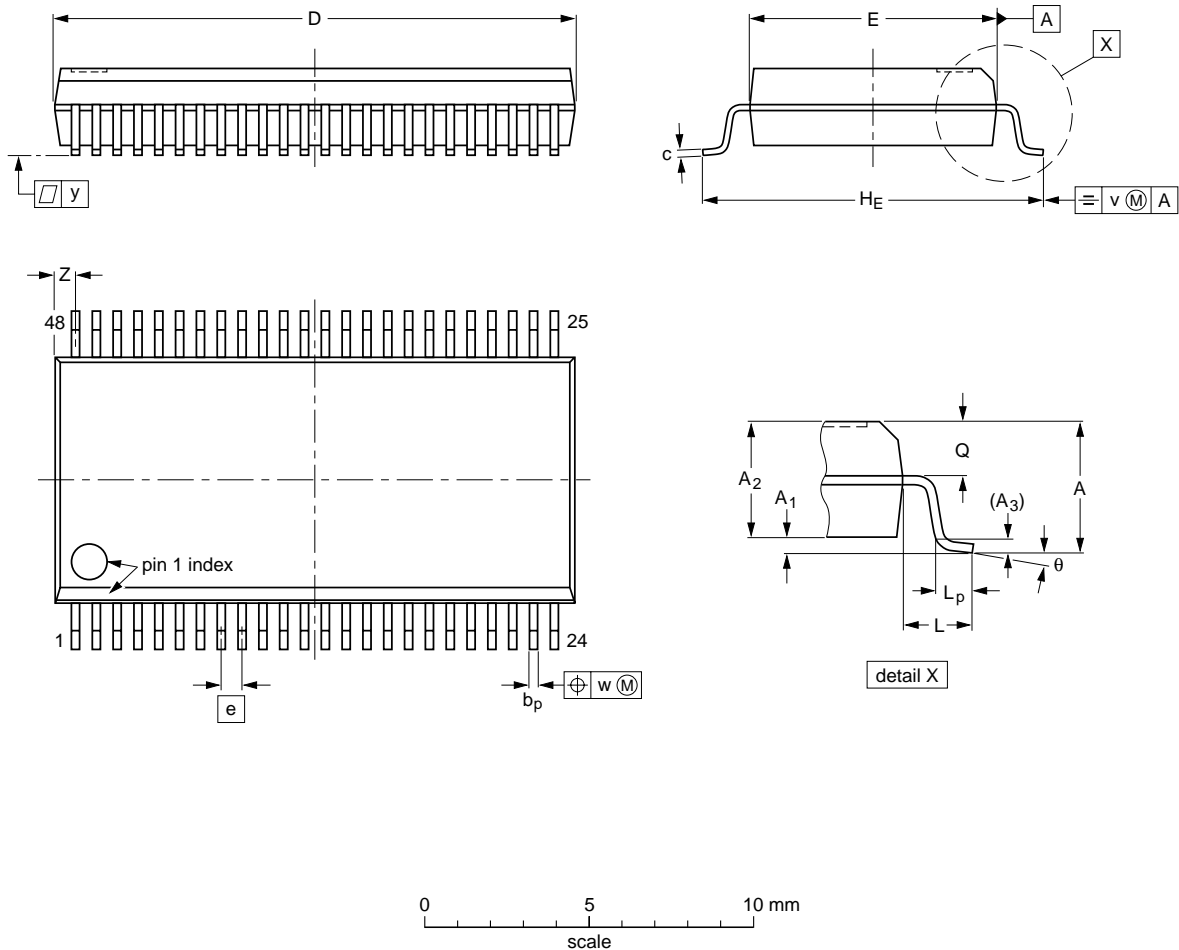
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**PACKAGE OUTLINES**

**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm**

**SOT370-1**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v    | w    | y   | z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm   | 2.8    | 0.4<br>0.2     | 2.35<br>2.20   | 0.25           | 0.3<br>0.2     | 0.22<br>0.13 | 16.00<br>15.75   | 7.6<br>7.4       | 0.635 | 10.4<br>10.1   | 1.4 | 1.0<br>0.6     | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40     | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

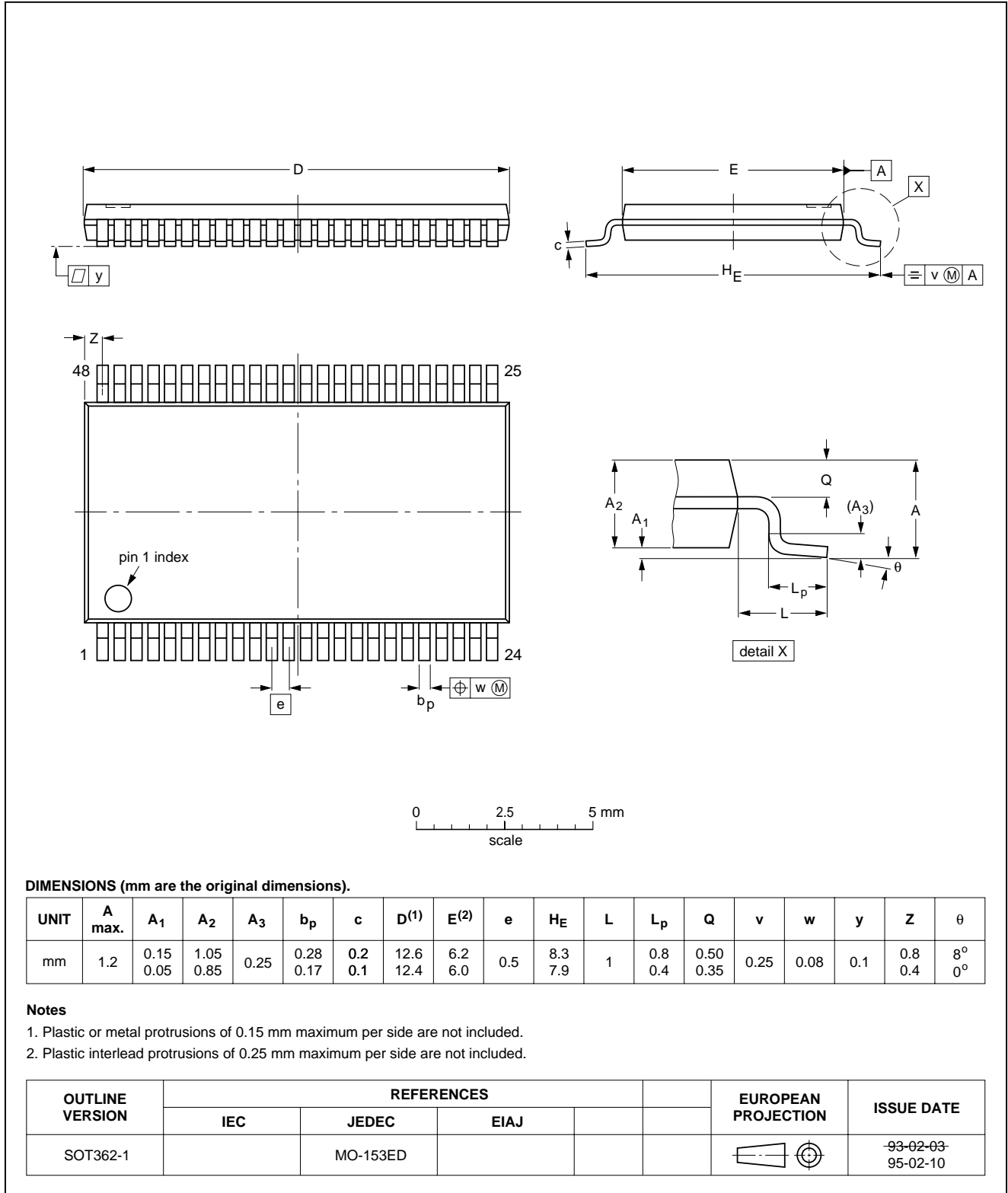
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT370-1        |            | MO-118AA |      |  |                     | 93-11-02<br>95-02-04 |

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



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## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16-bit D-type transparent latch with 30  $\Omega$  series  
termination resistors; 5 V input/output tolerant; 3-state

74LVC162373A;  
74LVCH162373A

#### Suitability of surface mount IC packages for wave and reflow soldering methods

| PACKAGE                       | SOLDERING METHOD                  |                       |
|-------------------------------|-----------------------------------|-----------------------|
|                               | WAVE                              | REFLOW <sup>(1)</sup> |
| BGA, SQFP                     | not suitable                      | suitable              |
| HLQFP, HSQFP, HSOP, SMS       | not suitable <sup>(2)</sup>       | suitable              |
| PLCC <sup>(3)</sup> , SO, SOJ | suitable                          | suitable              |
| LQFP, QFP, TQFP               | not recommended <sup>(3)(4)</sup> | suitable              |
| SSOP, TSSOP, VSO              | not recommended <sup>(5)</sup>    | suitable              |

#### Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

#### DEFINITIONS

| Data sheet status   |   |
|---|---|
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| Limiting values   |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| Application information   |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),  
Tel. +39 039 203 6838, Fax +39 039 203 6800

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,  
Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 62 5344, Fax.+381 11 63 5777

**For all other countries apply to:** Philips Semiconductors,  
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,  
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

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